

REMARKS

Claims 1-32 are pending and claims 1-27 are rejected. Claims 1, 17, and 25 are amended. Claims 28-32 are newly added. No new matter is added.

First 35 U.S.C. §103 Rejection

Claims 1-2, 5, 17-21, and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitten (U.S. Patent No. 5,805,795) in view of Bening (“Optimizing Multiple EDA Tools within the ASIC Design Flow”).

Whitten discloses methods, computer program products, computer systems, and apparatuses for testing software products (col. 1, lines 10-12). In these methods, the ultimate goal is to derive a subset of test cases that exercises a maximum number of the identified code blocks in a minimum amount of time (col. 5, lines 45-48). Accordingly, in a data base 19, a test case "A" is shown to have a execution time of 20 minutes, and executes blocks 1, 2, and 24 (col. 5, lines 53-55). A test case "B" is shown to have a execution time of 5 minutes, and executes blocks 1, 3, 19, and 24 (col. 5, lines 58-60). It may be observed, for instance, that test cases "A" and "B" both execute blocks 1 and 24, so an opportunity may exist to select one or the other test case, for example, test case "B" to minimize run time for testing these common blocks, if coverage can be obtained elsewhere for block 2 in test case "A" (col. 5, lines 60-65).

Bening discloses that a method for optimizing multiple electronic design automation (EDA) tools within an application specific integrated circuit (ASIC) design flow. The method includes developing a coding style and a design flow methodology that incorporates modern programming language principles (page 46, first column). The method further includes developing a design methodology to automate generation of tool-specific libraries (page 46, first column). The method supports a register transfer level (RTL) reuse by identifying a common set of RTL functional text-macro objects and creating a generic Verilog library describing functional behavior of each text macro-object (page 51, first column-second column).

Applicants respectfully submit that neither Whitten nor Bening, considered alone or in combination, disclose or suggest a method as called for by claim 1. For example, the combination of Whitten and Bening does not disclose or suggest “determining whether a predetermined number of the test designs for testing the design automation tool has been generated”. The specification provides an

example of this feature in a statement that “[a]t 517, it is determined if the required number of designs have been generated” (page 15, lines 4-5).

Whitten discloses satisfying an ultimate goal of deriving a subset of test cases that exercises a maximum number of code blocks in a minimum amount of time and Bening discloses supporting a register transfer level (RTL) reuse by identifying a common set of RTL functional text-macro objects and creating a generic Verilog library describing functional behavior of each text macro-object. The ultimate goal in Whitten of deriving a subset of test cases teaches away from determining whether a predetermined number of test designs has been generated. The subset of test cases in Whitten are not predetermined because they are derived to exercise a maximum number of code blocks in a maximum number of time. Hence, for at least these reasons, claim 1 would not have been obvious over the combination of Whitten and Bening.

Moreover, Whitten and Bening either alone or in combination do not relate to testing a design automation tool as recited in the independent claims. Rather, Whitten relates to methods, computer program products, computer systems, and apparatuses for testing software products and Bening relates to a method for optimizing multiple electronic design automation (EDA) tools within an application specific integrated circuit (ASIC) design flow. The method of Bening includes developing a coding style and a design flow methodology that incorporates modern programming language principles. The method of Bening further includes developing a design methodology to automate generation of tool-specific libraries. The testing of a computer program product in Whitten does not disclose or suggest testing a design automation tool and the optimization in Bening does not disclose or suggest testing.

The dependent claims, include, by virtue of their dependency, the features of the independent claims on which they are based. As such, the dependent claims would not have been obvious for at least the same reasons as their respective independent claims.

Therefore, for at least the reasons set forth above, Applicants respectfully request that the Section 103 rejection of Claims 1-2, 5, 17-21, and 25-27 be withdrawn.

Second 35 U.S.C. §103 Rejection

Claims 4, 6-13, 15, and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitten in view of Bening and in further view of Zaidi (2002/0038401 A1).

Zaidi discloses a simulation environment that is modeled after how a user design might appear in a system. A top level testbench is defined in a file “sim.env” located in a “chip/sim/” directory (paragraph 48). Such file includes several files to handle different aspects of the simulation environment (paragraph 48).

Claims 4, 6-13, and 15 depend from independent claim 1. As explained above, the combination of Whitten and Bening does not disclose or suggest a method as recited in claim 1. Zaidi discloses using a testbench, which, in combination with the other cited art, does not teach or suggest “determining whether a predetermined number of the test designs for testing the design automation tool has been generated” as called for by claim 1. Accordingly, for at least these reasons, claims 4, 6-13, and 15 would not have been obvious over the combination of Whitten, Bening, and Zaidi.

For at least the reasons set forth above, Applicant respectfully submits that the combination of Whitten, Bening, and Zaidi does not disclose or suggest a computer system as recited in claim 17 and dependent claims 22-24. Accordingly, claims 22-24 would not have been obvious over the combination of Whitten, Bening, and Zaidi.

Third 35 U.S.C. §103 Rejection

Claims 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Whitten in view of Bening and Zaidi and in further view of Goossens (“Design of Heterogeneous ICs for Mobile and Personal Communication System”).

Claims 14 and 16 depend from independent claim 1. As explained above, the combination of Whitten, Bening, and Zaidi does not disclose or suggest a method as recited in claim 1. Moreover, Goossens is not cited to address the deficiencies mentioned above with respect to Whitten and Bening. For example, Goossens is cited to teach “submodules comprising of adders and phase lock loops” and “clock structures that include a plurality of synchronous and asynchronous structures” (Office Action, page 7). Accordingly, for at least these reasons, claims 14 and 16 would not have been obvious over the combination of Whitten, Bening, and Goossens.

Fourth 35 U.S.C. §103 Rejection

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Whitten in view of Bening and in further view of Rajsuman (U.S. Patent No. 6,678,645).

Claim 3 depends from independent claim 1. As explained above, the combination of Whitten and Bening does not disclose or suggest a method as recited in claim 1. Moreover, Rajsuman is not cited to address the deficiencies mentioned above with respect to Whitten and Bening. For example, Rajsuman is cited to teach “generating a plurality of test designs of an ASIC including DSP and memory submodules” (Office Action, page 8). Accordingly, for at least these reasons, claim 3 would not have been obvious over the combination of Whitten, Bening, and Rajsuman.

New Claims

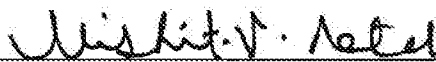
Claims 28-29 depend from independent claim 1, claims 30-31 depend from independent claim 17, and claim 32 depends from independent claim 25. As explained above, claims 1, 17, and 25 would not have been obvious over the cited art. Accordingly, Applicant respectfully submits that claims 28-32 would not have been obvious over the cited art.

Conclusion

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicants believe that all pending claims are allowable in their present form. Please feel free to contact the undersigned at the number provided below if there are any questions, concerns, or remaining issues.

Respectfully submitted,
/G. Audrey Kwan/
G. Audrey Kwan
Reg. No. 46,850

Respectfully submitted,



Nishitkumar V. Patel
Reg. No. 65,546

Weaver, Austin, Villeneuve, and Sampson LLP
P.O. Box 70250
Oakland, CA 94612-0250
(510) 663-1100